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I. Earned Degrees

Degree	*School*	*Date*	*Major*
Ph.D.	University of California at Berkeley	1992	EECS
M.S.	University of California at Berkeley	1990	EECS
B.S.	Pratt Institute (Honors)	1985	EE

II. Employment

2022 – present	Eugene DeLoatch Endowed Professor in IoT, Morgan State University
2018 – present	Director, Cybersecurity & Policy (CAP) Center, Morgan State University
2016 – 2022	IoT Security Professor, Morgan State University
2012 – 2016	Professor, Morgan State University
2005 - 2012	Motorola Foundation Professor, School of ECE, Georgia Tech
2000 - 2005	Associate Professor, School of ECE, Cornell University
1998 - 2000	Assistant Professor, School of ECE, Cornell University
1997 - 1998	Dr. Martin L. King Visiting Professor, EECS Dept., MIT
1994 - 1997	Assistant Professor, School of ECE, Purdue University
1992 - 1994	Research Staff Member, IBM T. J Watson Research Center
1985 - 1986	Member of Technical Staff, AT&T Bell Laboratories

III. Summary Table

1) # of Ph.D. students advised as Committee Chair	**32**
2) # MS students advised	**40**
3) # of Ph.D. students currently advising	**12**
4) # of grants earned as PI and $ amount	**61 / $13.4M**
5) # of grants earned as Co-PI and $ amount	**3 / $1.5M**
6) # of different classes / # of total classes.	**8 / 54**
7) # of journal publications	**34**
8) # of conference publications	**103**
9) # of US patents	**8**

IV. Honors & Awards

- National Academies of Sciences, Engineering, and Medicine Army Science and Technology Roundtable
- National Institute of Standards and Technology IoT Advisory Board Member, 2022 -present.
- Sigma Xi Scientific Research Honor Society, 2021 – present.
- Black Engineer of the Year Innovation Award, US Black Engineer Magazine, February 2018.
- State of Maryland Cybersecurity Council Member, 2017 – present.

- 2006 IBM Faculty Award
- Named Science Spectrum Trailblazer by Science Spectrum Magazine, 2005.
- Member Profile Feature in *IEEE Institute* June 2005.
- 2005 Golden Torch Award for Educator of the Year from the National Society of Black Engineers.
- Guest Editor, Special Issue of the IEEE Journal of Solid State Circuits: Compound Semiconductor IC Symposium, 2005.
- 2004 IEEE Bipolar/BiCMOS Circuits and Technology Meeting Best Student Paper Award (Student: D. Guckenberger, Advisor: K. Kornegay).
- Featured in *Science Spectrum* and *US Black Engineer & Information Technology* magazines as one of 50 Most Important Blacks in Research Science, 2004.
- 2004 Menschel Award, Cornell University Provost's Award for Distinguished Scholarship.
- IBM Faculty Award, 2001-2005.
- 2003 IEEE Electron Devices Society George Smith Award Finalist.
- 2003 Device Research Conference Best Student Paper Award (Student: D. Fried, Advisor: K. Kornegay).
- World Champion, 6th International Underwater Vehicle Competition, sponsored by the Association for Unmanned Vehicle Systems Corporation, 2003.
- 3rd Place Winner, , Semiconductor Research Corporation Silicon Germanium (SiGe) Design Challenge, (59 universities competed), 2003.
- Featured at the Chicago Museum of Science and Industry as part of an exhibit showcasing contributions made by African Americans to the field of information technology, 2003.
- Invited Attendee, 5th German-American Symposium on Frontiers of Engineering, National Academy of Engineering, 2002.
- Black Engineer of the Year Award in Higher Education, US Black Engineer Magazine, 2002.
- Defense Sciences Study Group, Institute for Defense Analyses/DARPA, 2002-2003.
- Invited Attendee, 5th Annual Symposium on Frontiers of Engineering, National Academy of Engineering, 1999.
- National Science Foundation CAREER Award, 1999.
- MIT Dr. Martin Luther King, Jr. Visiting Assistant Professor, 1997.
- Harold T. Amrine Visionary Award from the National Society of Black Engineers, 1997.
- Elected IEEE Senior Member, 1996.
- National Semiconductor Faculty Development Award (Inaugural Recipient), 1996.
- General Motors Faculty Fellowship, 1995.
- AT&T Bell Laboratories Cooperative Research Fellowship, 1986 - 1992.
- AT&T Scholarship, 1983 - 1986.
- Eta Kappa Nu Electrical Engineering Honor Society.
- Tau Beta Pi Engineering Honor Society.

V. Teaching/Advising

A. Ph.D./Doctorate Student Guidance as Thesis Committee Chair

Purdue University School of Electrical and Computer Engineering

Name	Ph.D. Dissertation Title	Graduation Date	Place of Employment
1. Sei-Hyung Ryu	Development of CMOS Technology for Smart Power Application in Silicon Carbide	Spring 1997	Chief Scientist, Wolfspeed, Durham, NC
2. Jian-Song Chen	Analog Integrated Circuit Technology using 6H Silicon Carbide CMOS Technology	Fall 1997	Texas Instruments Inc., Dallas, TX
3. Man Pio Lam	Development of Submicron CMOS in 6H-SiC	Spring 1998	Hitachi Corp., Santa Clara, CA

Cornell University School of Electrical and Computer Engineering

Name	Ph.D. Dissertation Title	Graduation Date	Place of Employment
1. Andrew Atwell	Silicon Carbide MEMS Devices for Harsh Environments	Fall 2002	Research Staff Member, Institute of Defense Analysis, Centreville, VA
2. Eskinder Hailu	Monolithic Integration of Electronics and MEMS in Silicon Carbide for Use in Harsh Environments	Fall 2002	Principal Engineer, High-speed I/O, Intel Corp, Raleigh, NC
3. Ce Li	Silicon Carbide Nonvolatile Memory for Harsh Environments	Spring 2003	Patent Attorney, Washington, DC
4. Mihaela Balsenu	Silicon-on-Silicon System Packaging	Spring 2003	Corporate Director, ASM, Netherlands
5. Swaroop Kumar Kommera	Seamless Tiling of Silicon Dies for Micro-Display Applications and Novel Structures for On-chip Power and Ground Distribution	Fall 2003	IBM Corp, Burlington, VT
6. Paul Ampadu **(IBM PhD Fellow)**	An Energy Efficient Approach to 3G Turbo Decoding	Spring 2004	Professor, ECE, VaTech, Innovation Campus, VA

7. David Fried IBM PhD Fellow	The Design, Fabrication, and Characterization of Independent Gate FinFETs	Spring 2004	VP at Lam Research, Los Gatos, CA.
8. J. C. Zhan	Design of Emitter Degenerated Voltage Controlled Oscillators	Spring 2004	Manager, MediaTek, Hsinchu City, Taiwan
9. Sean Welch **(Intel PhD Fellow)**	Design and Analysis of an Improved Clocking Methodology for Next-generation Physically Aware Synchronous Architectures	Spring 2004	Staff Engineer, Intel Corp, , MA.

10. Ian Rippke	Design and Analysis of an Improved	Spring 2005	Keysight Technologies, Allentown, PA
11. Kyle Maurice	Clocking Methodology for Next-generation Physically Aware Synchronous Architectures	Spring 2005	Data Scientist, Intel Corp., Hillsboro, OR.
12. Franklin Baez	The Modeling and Design of a Multi-Standard Frequency Synthesis System	Spring 2005	Packaging Engineer, IBM Corp., East Fishkill, NY
13. Drew Guckenberger **(IBM PhD Fellow)**	Low Power Analog Baseband for WCDMA Wireless Receivers	Spring 2005	VP, High-Speed Interconnect, Maxlinear, San Diego, CA.
14. Daniel Kucharski **(IBM PhD Fellow)**	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Spring 2005	Sr. Principal Engineer, Sematech, San Diego, CA
15. Brian Welch **(IBM PhD Fellow)**	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Spring 2005	Director of Product Marketing, Luxtera, Carlsbad, CA.

16. Yanxin Wang	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Fall 2006	Principal Design Scientist, Broadcom., Carlsbad, CA.
17. Javier Alvarado **(Intel PhD Fellow)**	Low-power Integrated Silicon Optical Receiver Design for High-Performance Datalinks	Fall 2006	Raytheon Technologies, Arlington, VA.
18. Pukar Malla **(Intel PhD Fellow)**	Cognitive Delta-Sigma ADC Design for Smart Power Adaptive Digitally Enhanced Receivers	Fall 2007	Founder, Nepal Leadership Academy, Nepal.

Georgia Tech School of Electrical and Computer Engineering

Name	**Ph.D. Dissertation Title**	**Graduation Date**	**Place of Employment**
1. Tonmoy Mukherjee	High-Performance, Robust, Multi-Gigabit Wireline Design	May 2010	Sr. Director, Marvell Technology, Los Angeles, CA.
2. Jihwan Kim	CMOS PA Design	May 2011	Sr. Staff Engineer, Intel Corp., Hillsboro, OR
3. Eung Kim	CMOS Switch Design	May 2011	Qualcomm Inc., San Diego, CA

Morgan State University Department of Electrical and Computer Engineering

Name	**Ph.D. Dissertation Title**	**Graduation Date**	**Place of Employment**
1. Hailu Belay (Kassa)	Adaptive Energy Efficient Cellular Networks	Dec. 14, 2018	CAP Center Research Engineer
2. Marcial Tienteu	Side-Channel Resiliency Analysis of Embedded Systems	May 18, 2023	Consultant
3. Khir Henderson **(2018 GEM PhD Fellow, Sponsor: JHU Applied Physics Lab)**	Designing a Sustainable and Secure Network Security Architecture for the Internet of Things	May 19, 2022	HarborLabs, Pikesville, MD.

4. Denzel Hamilton **(2018 GEM PhD Fellow, Sponsor: JHUAPL)**	Exploring Explainable AI for Autonomous Vehicle Assurance	May 19, 2022	Johns Hopkins Applied Physics Laboratory, Laurel, MD.
5. Edmund Smith **(2018 GEM Associate PhD Fellow, NIST PREP)**	Light Weight Cryptography for Embedded Systems	May 18, 2023	Sandia National Laboratories, Albuquerque, NM.
6. Sean Richardson **(Verizon)**	IoT Security for 5G Networks	May 18,2023	Verizon
7. Tsion Yimer (**MITRE Scholar**)	Vulnerability Assessment and Mitigation for Physical Attacks on Building Automation Control Networks (BACKNET) Systems	May19, 2022	The MITRE Corp, McLean, VA.
8. Otily Toutsop (**NIST PREP**)	Internet of Things Platform Security and Countermeasures	May 19, 2022	NIST, Gaithersburg, MD.
9. Paige Harvey **DoD Cybersecurity Scholar**	Medical IoT Device Security	May 18, 2023	NSA, Fort Meade, MD.
10. Arron Edmund **DoD Cybersecurity Scholar**	MS in Secure Embedded Systems	May 19, 2021	Navy Information Warfare Center Atlantic, Charleston, SC.
11. Caroline Kinyanjui **CAP Scholar**	Hardware Security	TBD	NIST PREP Intern.
12. Gregory Briscoe **CAP Scholar**	Secure Autonomous Navigation	TBD	TBD
13. Robert Hill **CAP Scholar**	Hardware Security	TBD	TBD
14. Shelanice Clash **NSF CyberCorps Scholar**	Adversarial Artificial Intelligence	May 2024	NSA, Fort Meade, MD.

15. Ahamed Jemal **CAP Scholar**	Blockchain Applications in IoT Security	TBD	TBD
16. Loic Jephson Djomo Tchuenkou **CAP Scholar**	Hardware Reverse Engineering	TBD	TBD
17. Joy Falaye **NSF CyberCorp Scholar**	IoT Security	TBD	TBD
18. Jose Domingues Cortez **CAP Scholar**	Secure SoC Design	TBD	TBD
19. Rachida Kone **NSF CyberCorps Scholar**	Adversarial AI	May 2024	DISA, Norfolk, VA.
20. German Cortes	mmW Gan Power Amplifier Design	Summer 2024	ARL, Aberdeed, MD.
21. Alemayehu Kassa	Home IoT Device Security	TBD	TBD
22. Vinton Morris	Security for Zero Trust Networks	TBD	TBD

B. Undergraduate Student Guidance

Morgan State University Department of Electrical and Computer Engineering

Name	**Senior Design Project Title**	**Graduation Date**
1. Paige Harvey	Secure Boot on a Xilinx Zedboard	May 2018
2. Sydney Johns	Controller Area Network Application Board Vulnerabilities	May 2018
3. Saxfield Chatmon	Controller Area Network Application Board Countermeasures	May 2018

3. Jerell Culberson	Hacking an ARM based Processor Application Board using Simple Power Attacks	May 2018
4. Malaika Wanjihia	Secure Embedded Systems	Dec 2020
5. Nafetalia Fifita	Side Channel Resistance Analysis	Dec 2020
6. Jeremiah Conway	Secure SoC Design	May 2024
7. Keyann _Wekan-Kemeni	Side-Channel Analysis	May 2027
8. Hillary Binda	Embedded System Design	May 2027

Courses (UG = Undergraduate/G = Graduate)

- Digital IC Design (UG Tape out class)
- RFIC Design (G)
- Mixed-Signal Amplifier Design (UG)
- Microelectronic Circuits (UG)
- Adv VLSI Design (G)
- Advanced Hardware Security (G)

VI. Scholarly Accomplishments

A. Books and Parts of Books

K. T. Kornegay, "Chip and Board Testing," Chapter 14 in book entitled "Anatomy of a Silicon Compiler," Edited by R.W. Brodersen, *Kluwer Academic Publishers*, Norwell, MA, pp.187-196, 1992.

Kevin Kornegay, "Perception of Cyber Threats, " Chapter 4 in book entitled "Autonomous Intelligent Cyber Defense Agent," Edited by Alexander Kott, Springer, pp. 63-78, 2023.

B. Refereed Publications

*The boldface font is used to identify doctoral student co-authors.

Journal Publications

[J1] K. T. Kornegay and R. W. Brodersen, "Integrated Test Solutions for a System Design Environment," *J. VLSI Design*, vol. 1, pp. 345-357, Jan. 1994.

[J2] **S. Ryu** and K. T. Kornegay, "Design and Fabrication of Depletion Load NMOS Integrated Circuits in 6H-SiC," *Proc. Int. Conf. Silicon Carbide and Related Mater*., pp. 789-792*,* Feb.1996.

[J3] K. T. Kornegay and K. Roy, "Structured Test Methodologies and Test Economics for Multichip Modules," *IEEE Trans. Compon. Packag. Technol.*, vol. 19, pp. 195-202, Feb. 1996.

[J4] **J. Chen** and K. T. Kornegay, "Class AB CMOS Power OPAMP with Stable Voltage Gain over a Wide Temperature Range," *IEE Proc., Circuits Devices Syst.,* vol. 144, pp. 22-28*,* Feb.1997.

[J5] **M. P. Lam**, K. T. Kornegay, J.A. Cooper, Jr. and M. R. Melloch, "Planar 6H-SiC MESFETs with Vanadium Implanted Channel Termination," *IEEE Trans. Electron Devices,* vol. 44, pp. 907-910, May 1997.

[J6] **S. Ryu**, K. T. Kornegay, J.A. Cooper, Jr., and M. R. Melloch, "Monolithic CMOS Digital Integrated Circuits in 6H-SiC Using an Implanted P-Well Process," *IEEE Electron Device Lett.,* vol. 18, pp. 194-196, May1997.

[J7] **S. Ryu**, K. T. Kornegay, J. A. Cooper, Jr., and M R. Melloch, "Digital CMOS ICs in 6H-SiC Operating on a 5V Power Supply," *IEEE Trans. Electron Devices,* vol. 45, pp. 45-53*,* Jan. 1998.

[J8] **M. P. Lam**, M. K. Das, J. N. Pan, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Effects of Nitrogen Implant Activation on the SiC/SiO_2 Oxide Interface of 6H-SiC Self-Aligned Mosfets," *IEEE Trans. Electron Devices,* vol. 45, pp. 565-567*,* Feb. 1998.

[J9] **J. Chen** and K. T. Kornegay, "Design of a Process Variation Tolerant CMOS OPAMP in 6H-SiC Technology for High Temperature Operation," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 1159-1171, Nov. 1998.

[J10] I. Hong, D. Kirovski, K. T. Kornegay and M. Potkonjak, "High-Level Synthesis Techniques for Test Pattern Execution," *Integ. VLSI J.,* vol. 25, pp. 161-180, Nov. 1998.

[J11] **J. Chen**, K. T. Kornegay, and S. Ryu, "A Silicon Carbide CMOS Intelligent Gate Driver Circuit with Stable Operation over a Wide Temperature Range," *IEEE J. Solid-State Circuits,* vol. 34, pp. 192-204, Feb. 1999.

[J12] **M. P. Lam** and K. T. Kornegay, "Recent Progress in 6H-SiC CMOS Devices for Smart Power Applications," *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 546-554, March 1999.

[J13] **M. P. Lam** and K. T. Kornegay, "Punchthrough Behavior in Short Channel 6H-SiC MOS Transistors at Elevated Temperatures," *IEEE Trans. Compon. Packag. Technol.,* vol. 22, pp. 433-438, Sept. 1999.

[J14] G. L. Katulka, D. J. Hepner, B. Davis, E. Irwin, M. Ridgley, and K. T. Kornegay, "Characterization of Silicon Carbide and Commercial-Off-The-Shelf (COTS) Components for High-g Launch and EM Applications," *IEEE Trans. Magnetics*, vol. 37, pp. 248-251,

Jan. 2001.

[J15] **A. Atwell**, R. Okojie, K. Kornegay, S. Roberson and A. Beliveau, "Simulation and Validation of Bulk Micromachined 6H-SiC High-G Piezoresistive Accelerometers," *IEEE Sens. Actuators A*, *Phys.*, vol. 104, pp. 11-18, Feb. 2003.

[J16] **C. Li**, J. S. Duster and K. Kornegay, "A Nonvolatile Memory Device in 6H-SiC for Harsh Environment Applications," *IEEE Electron Device Lett.,* vol. 24, pp. 72-74, Feb. 2003.

[J17] **J. C. Zhan**, K. Maurice, J. S. Duster and K. T. Kornegay, "Analysis and Design of Negative Impedance LC Oscillators Using Bipolar Technology," *IEEE Trans. Circuits Syst. I*, vol. 50, Nov. 2003.

[J18] **D. M. Fried**, J. S. Duster, and K. T. Kornegay, "High Performance P-Type Independent-Gate FinFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 199-201, April 2004.

[J19] **J. C. Zhan**, J. S. Duster and K. T. Kornegay, "Design of Negative Impedance LC Oscillators using Bipolar Technology," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2062-64, Nov. 2004.

[J20] **D. Kucharski** and K. T. Kornegay, "Jitter Considerations in the Design of a 10 Gb/s Automatic Gain Control Amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 53, pp. 590-597, Feb. 2005.

[J21] **J. C. Zhan**, J. S. Duster, and K. T. Kornegay, "A high f_{osc}/f_T Ratio VCO in SiGe BiCMOS Technology," *IEEE Microw. Wirel. Comp. Lett.*, vol. 15, pp. 149-161, March 2005.

[J22] **D. Guckenberger**, C. Shuster, Y. Kwark, and K. T. Kornegay, "On-chip Crosstalk Mitigation of Densely Packed Striplines using via Fence Enclosures," *Electron. Lett.*, vol. 41, pp. 412-414, March 2005.

[J23] **D. Guckenberger** and K. T. Kornegay, "Design of a Distributed Amplifier and Oscillator using Closed-packed Interleaved Transmission Lines," *Special Issue on the IEEE 2004 BCTM*, *IEEE J. Solid-State Circuits,* vol. 40, pp. 1997-2007, Oct. 2005.

[J24] **B. Welch**, K. Kornegay, H. Park, and J. Laskar, "A 20 GHz Low Noise Amplifier with Active Balun in a 0.25 μm SiGe BICMOS technology," *Special Issue on the IEEE 2004 CSICS*, *IEEE J. Solid-State Circuits,* vol. 40, pp.2092-2097*,* Oct. 2005.

[J25] **D. Kucharski** and K. Kornegay, "A 2.5V 43-45 Gb/s CDR Circuit and 50 Gb/s PRBS Generator in SiGe using a Low Voltage Logic Design Family," *Special Issue on the IEEE 2005 BCTM*, *IEEE J. Solid-State Circuits,* vol. 41, pp. 2154-2165, Sept. 2006.

[J27] **T. S. Mukherjee**, A. K. Sutton, K. T. Kornegay, R. Krithivasan, J. D. Cressler, G. Niu, and P. W. Marshall, "A Novel Circuit-Level SEU Hardening Technique for High-Speed SiGe HBT Logic Circuits," *IEEE Trans. on Nuclear Sci*., vol. 54, pp. 2086-2091, Dec. 2007.

[J28] **P. Malla**, H. Lakdawala, R. Naiknaware, S. Krishnamurthy, and K. Kornegay, "Delta Sigma ADC Design Considerations for WiFi/WiMAX Receivers," *Analog Integrated Circuits and Signal Processing Journal*, 2008.

[J29] **J. Kim**, K.T. Kornegay, J.A. Alvarado, C.H. Lee, and J. Laskar, "W-band double-balanced down-conversion mixer with marchand baluns in silicon-germanium technology," *Electronics Letters*, vol.45, no. 16, pp. 841-843, July 2009.

[J30] **J. Kim**, H. Kim, Y. Yoon, K. H. An, W. Kim, C.-H. Lee, and K. T. Kornegay, "A Linear Multi-Mode CMOS Power Amplifier with Discrete Resizing and Concurrent Power Combining Structure, to appear in*, IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1034-1048, June 2011.

[J30] J. Kim **J. Kim**, H. Kim, Y. Yoon, K. H. An, W. Kim, C.-H. Lee, and K. T. Kornegay, "A Fully-Integrated High-Power Linear CMOS Power Amplifier with a Parallel-Series Combining Transformer," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 599-614, March 2012.

[J31] T. Kebede, Y. Wondie, J. Steinbrunn, H. Belay and K. Kornegay, "Precoding and Beamforming Techniques in mmWave-Massive MIMO: Performance Assessment," in *IEEE Access*, doi: 10.1109/ACCESS.2022.3149301.

[J32] T. Kebede, Y. Wondie, J. Steinbrunn, H. Belay and K. Kornegay, " Multi-carrier Waveforms and Multiple Access Strategies in Wireless Networks: Performance, Applications and Challenges," in *IEEE Access*, doi: 10.1109/ACCESS.2022.3151360.

[J33] Aredo S.C., Negash Y., Marye Y.W., Kassa H.B., Kornegay K.T., Diba, F.D. "Hardware Efficient Massive MIMO Systems with Optimal Antenna Selection," in *Sensors*. 2022; 22(5):1743. https://doi.org/10.3390/s22051743.

[J34] Bailey, D., & Kornegay, M. A., & Partlow, L., & Bowens, C., & Gareis, K., & Kornegay, K., "*Utilizing Culturally Responsive Strategies to Inspire African American Female Participation in Cybersecurity*," to appear in Journal of Pre-College Engineering Education Research (J-PEER), Oct. 2023.

Refereed Conference Publications

[C1] A. Stolzle, S. Narayanaswamy, K. T. Kornegay, et al., "A VLSI Implementation for the Wordprocessing Subsystem of a Real-Time Large Vocabulary Continuous Speech Recognition System," *Proc*. *IEEE CICC*, 1989, pp.15-18.

[C2] K. T. Kornegay and R. W. Brodersen, "A Test Controller Board for TSS," *Proc*. *Great Lakes Symp. VLSI*, 1991, pp. 38-42.

[C3] K. T. Kornegay and R. W. Brodersen, "An Architecture for a Reconfigurable IEEE 1149.1,2, or 5 Master Controller Board," *Proc*. *IEEE Int. Test Conf.*, 1992, pp. 978-983.

[C4] M. Potkonjak, S. Dey and K. T. Kornegay, "Techniques for Implementation of At-Speed Testable, High Performance, and Low Cost Linear Designs," presented at the 1995 *Int. Test Synth. Workshop*, May 1995.

[C5] **S. Ryu** and K. T. Kornegay, "Design and Fabrication of Depletion Load NMOS Integrated Circuits in 6H-SiC," *Proc. Int. Conf. Silicon Carbide and Related Mater.*, 1995, pp. 475-476.

[C6] M. Potkonjak, S. Dey and K. T. Kornegay, "Techniques for Implementation of At-Speed Testable, High Performance and Low Cost Linear Design," *Proc. VLSI Signal Processing*, 1995, pp. 227-236.

[C7] K. T. Kornegay and K. Roy, "Integrated Test Solutions and Test Economics for MCMs,"

Proc. IEEE Int. Test Conf., 1995*,* pp. 193-201.

[C8] **M. P. Lam**, K. T. Kornegay and J. A. Cooper, Jr., "A Highly Resistive Layer in Silicon-Carbide Obtained by Vanadium Ion Implantation," *Proc. Int. Semicond. Device Res. Symp.*, 1995, pp. 517-519.

[C9] L. Chiou, K. M. Mahoney, K. T. Kornegay and A. M. Weiner, "High-Speed Switching Circuits for Ultrafast Optical Processing," *Proc. IEEE Int. Symp. Circuits Syst., 1996,* pp. 109-112.

[C10] **M. P. Lam**, K. T. Kornegay, J.A. Cooper, Jr., and M. R. Melloch, "Ion Implantation Technology for 6H-SiC MESFET Digital ICs," *DRC Dig.,* 1996*,* pp. 158-159.

[C11] **J. Chen** and K. T. Kornegay, "Design of a Silicon Carbide CMOS Power OPAMP for Stable Operation at Elevated Temperatures," *Proc. IEEE ISCAS,* 1997*,* pp. 157-160.

[C12] **S. Ryu**, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "6H-SiC Digital CMOS ICs Operating on a 5V Power Supply," *DRC Dig.*, 1997, pp. 38-39.

[C13] **M. P. Lam**, K .T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Effects of Implant Anneal on Oxide Interface of Self-Aligned Mosfets in 6H-SiC," *EMC Dig. Tech. Papers*, 1997, pp. 27-28.

[C14] **J. Chen** and K. T. Kornegay, "Design of a Silicon Carbide Smart Power Switch with Stable Operation over a Wide Temperature Range," *Proc. IEEE Midwest Symp. Circuits Syst.*, 1998, pp. 123-126.

[C15] **J. Chen** and K.T. Kornegay, "A constant input gm and rail-to-rail CMOS OPAMP using 6H SiC CMOS technology," *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, pp. 241-244.

[C16] K.T. Kornegay, "Design Issues in Power Electronics Building Block (PEBB) System Integration," *Proc. IEEE Computer Society Workshop on VLSI*, 1998, pp. 48-52.

[C17] **J. Chen**, S. Ryu and K. T. Kornegay, "High Temperature Mixed-Signal ICs using Silicon Carbide CMOS Technology," in *Proc. Int. High Temp. Electron. Conf.*, 1998, pp. 292-295.

[C18] **J. Chen**, S. Ryu and K. T. Kornegay, "A Silicon Carbide CMOS Intelligent Gate Driver Circuit," *IEEE Industry Appl. Society Annual Meeting Dig.*, 1998, pp. 963-966.

[C19] K. T. Kornegay, "Submicron Silicon Carbide CMOS for Smartpower Applications," *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 1999, pp. 297-300.

[C20] K. T. Kornegay, "Silicon Carbide CMOS Technology for High Temperature Applications," *NASA/JPL Conf. Electron. Extreme Environ.*, 1999, pp. 14-18.

[C21] E. Eshun, C. Taylor, M. G. Spencer, K. T. Kornegay, I. Furgureson, and A. Gurray, "Homo-Epitaxial and Selective Area Growth of 4H and 6H Silicon Carbide using A Resistively Heated Vertical Reactor," *Proc. Symp. Bandgap Semicond. High-Power, High-Freq. High-Temp. Appl.*, 1999, pp. 173-179.

[C22] C. Thomas, C. Taylor, J. Griffen, M. G. Spencer, K. T. Kornegay, M. Capano, and S. Rendakova, "Annealing of Ion Implantation Damage in SiC using A Graphite Mask," in

Proc. Symp. Bandgap Semicond. High-Power, High-Freq. and High-Temp. Appl., 1999, pp. 45-50.

[C23] K. T. Kornegay, G. Qu, and M. Potkonjak, "Quality of Service and System Design," *Proc. IEEE Computer Society Workshop on VLSI*, 1999, pp. 112-117.

[C24] **S. M. Welch** and K. T. Kornegay, "Improved Synchronization Methodologies for High Performance Digital Systems," Invited Paper, *Proc. IEEE Computer Society Workshop on VLSI*, 2000, pp. 61-66.

[C25] **A. R. Atwell**, J. S. Duster, K. T. Kornegay, and R. S. Okojie, "A Novel CMOS-compatible Deep Etching Process for Silicon Carbide using Silicon Shadow Masks," *Proc. EMC*, June 2000.

[C26] **E. Hailu** and K. T. Kornegay, "Design of a Temperature Independent Current Source for High Temperature Operation," *Proc. Int. High Temp. Electron. Conf.*, May 2000.

[C27] K. T. Kornegay, "Anatomy of an RF Integrated Circuit Design Course," *Proc. IEEE Int. Conf. Microelectron. Syst. Educ.*, 2001, pp. 54-55.

[C28] R. S. Okojie, **A. R. Atwell**, K. T. Kornegay, S. L. Roberson, and A. Beliveau, "Design Considerations for Bulk Micromachined 6H SiC High-G Piezoresistive Accelerometers," *Proc. IEEE Int. Conf. MEMS Dig. Tech. Papers, 2002*, pp. 618-622.

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Patents

1. J. M. Woodall, K. T. Kornegay and M. G. Spencer, "Incandescent Light Energy Conversion with Reduced Infrared Emission," U.S. patent no. 5,814,840, issued September 29, 1998.
2. **D. Guckenberger**, K.T. Kornegay, "A Novel Low-Voltage Low-Power Transimpedance Amplifier Architecture," U.S. patent no. 7,042,295, issued May 9, 2006.
3. **D. Kucharski**, K.T. Kornegay, "Low-voltage high-speed differential logic devices and method of use thereof," U.S. patent no. 7,098,697, issued August 29, 2006.
4. K.T. Kornegay, et al., "Method for monolithically integrating silicon carbide microelectromechanical devices with electronic circuitry," U.S. patent no. 7,170,141, issued January 30, 2007.
5. **D. Kucharski**, K. Kornegay, "Extended bandwidth and oscillator using positive current feedback through inductive load," U.S. patent no. 7,215,194, issued May 8, 2007.
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8. H. Kassa, K.T. Kornegay, "Adaptive Energy-efficient Cellular Network," U.S. patent no. 11,240,752, issued February 1, 2022.

VII. Gifts, Grants, and Contracts

A. Purdue University (1995-1997), Cornell University (1998-2005), Georgia Tech (2005-2012

Sponsor	Period	Title	PI/Co-PI	Amount
1. NSF	11/95 - 5/96	A Look at Temperature Dependent Parameters for Digital Circuit Design Considerations using SiC MOSFET Technology	PI	$18,000
2. ONR	3/96 - 2/99	Design and Optimization of a SiC CMOS Process for Smart Power ICs	PI	$400,000
3. National Semiconductor	3/96 - 5/98	Faculty Development Award	PI	$40,000
4. Ballistic Missile Defense Organization	5/96 - 4/97	Instrumentation for Research on High Speed Optical Transmultiplexing and Coding	PI	$119,203

5. NSF	5/96 - 6/98	Hardware Prototyping Capability for a Community Service Projects Course in Electrical and Computer Engineering	PI	$159,310
6. ONR	4/97- 3/00	Microelectronic Integration and Test of PEBB Control Functions	PI	$300,000
7. Alcoa Foundation	5/98	Software and Hardware Infrastructure for High-Temperature Electronics	PI	$30,000
8. ONR	2/99 - 1/00	Silicon Carbide VLSI Technology	PI	$200,000
9. AFOSR	5/99 - 5/01	Stress Studies at High G-Loads using Silicon Carbide Piezoresistive Strain Gauges	PI	$200,000
10. NSF	7/99 - 6/03	CAREER Award: A Wireless Sensor Instrumentation System for Harsh Environments	PI	$400,000
11. DOE	8/99 - 7/00	Assessment of Silicon Carbide as a Viable Semiconductor for Development of High Temperature Electronics	PI	$15,000
12. AFRL/Wright Patterson Airforce	2/1/00 – 5/18/00	Fabrication of Silicon Carbide Pressure Sensors for Jet Engine Applications	PI	$27,000
13. Cadence	6/00	Donation: System Design Software for Cornell Broadband Communications Research Laboratory (CBCRL)	PI	Valued at $100,000,000
14. Digital/Compaq	6/00	Shared University Research Grant for Cornell Broadband Communications Research Laboratory (CBCRL)	PI	$750,000
15. Northrop Grumman	7/1/00 – 6/30/01	Improved Synchronization Methodologies for High Performance Digital Systems	PI	$30,000
16. NYSTAR - Alliance for Nanomedical Technologies	8/01-7/02	A Remote Non-invasive Ambulatory Patient Monitoring System	PI	$270,000
17. Northrop Grumman	12/1/00 – 12/31/00	Heterogeneous Integration of Silicon on Silicon	PI	$50,000
18. DARPA/MARCO	1/1/01 – 12/31/04	CCSS: A Collaborative Multi-University Research Center for Circuits, Systems & Software. 30 PIs from CMU, MIT, Stanford, UC-Berkeley, Columbia, Cornell, Princeton, RPI, and the University of Washington.	Co-PI	$18,747,993 (Kornegay: $380,000)
19. Agilent	1/01	Equipment Donation: 84000 Production RFIC Test System	PI	$1,200,000
20. Cascade Microtech	1/01	Equipment Donation: 8-inch Wafer Probe System	PI	$200,000
21. IBM Corp.	2/01	Gift for CBCRL	PI	$130,000
22. IBM Corp.	5/01	IBM Faculty Award	PI	$40,000

23. NYSTAR – Alliance for Nanomedical Technologies	8/01-7/02	A Remote Non-invasive Ambulatory Patient Monitoring System	PI	$270,000
24. IBM Corp.	5/02	IBM Faculty Award	PI	$40,000
25. NYSTAR – Microelectronics Design Research Center	8/1/02-7/31/03	Energy Efficient Turbo Decoders	PI	$50,000
26. Agilent	4/03	Gift for Laboratory Course Development	PI	$111,000
27. Intel Corp.	4/03	Research Award	PI	$65,000
28. SiGe Semiconductor	5/03	Power Amplifier Design	PI	$80,000
29. IBM Corp.	6/03	Faculty Award	PI	$50,000
30. Qualcomm Inc.	8/03	Gift for CBCRL	PI	$400,000
31. Cascade Microtech	12/03	Donation: 8 inch Wafer Probe System	PI	$200,000
32. Intel Corp.	12/03	CBCRL Equipment Donation	PI	$30,000
33. Intel Corp.	5/04	Research Award	PI	$65,000
34. IBM Corp.	6/04	Faculty Award	PI	$40,000
35. Analog Devices Inc.	8/04	Gift to Support CBCRL Research	PI	$50,000
36. Analog Devices	1/05	Gift to Support CBCRL Research	PI	$40,000
37. Intel Corp	5/05	Research Award	PI	$65,000
38. IBM Corp.	6/05	Faculty Award	PI	$25,000
39. Qualcomm Inc.	1/06	Gift for Research Support	PI	$30,000
40. IBM Corp.	6/06	Faculty Award	PI	$25,000
41. National Semiconductor Corp.	2/08	Very High-Speed Clock and Data Recovery Systems	PI	$50,000
42. National Semiconductor Corp.	1/09	Very High-Speed Clock and Data Recovery Systems	PI	$40,000
43. Korean Institute of Science and Technology	1/11-11/13	International Collaborative R&D Program: Development of a Fully Digital CMOS Transceiver IC for Mobile D-TV and Wireless Applications	PI	$617,000

B. Morgan State University (2012 – present)

44. Army	10/2014	Embedded Mobile Tactical Systems -- Reverse Engineering and Countermeasures (Equipment Grant)	PI	$212,000
45. NSF/HRD	4/1/2015-3/31/2018	RISE: Embedded Systems Security via Reverse Engineering and Countermeasures	PI	$999,450
46. Army Research Laboratory	9/25/2015 – 9/24/2020	IDIQ Contract: Design Techniques for Low Power Highly Linear CMOS Transceivers	PI	$3,099,906
47. IARPA	10/1/2016-9/30/2021	RAVEN: Nanoscale X-ray Tomosynthesis for Rapid Assessment of IC Dies (MIT Lead)	Co-PI	$12,000,000
48. DoD/NSA	5/1/2017-8/31/2017	NSA-LTS/Morgan State University Summer Cyber and Telecommunications Research	PI	$100,000
49. DoD/NSA	9/24/2017-9/23/2018	DoD Information Assurance Scholarship Program (IASP): CREAM Scholars and Capacity Building	PI	$212,636
50. DoD/NSA		DoD IASP: CREAM Scholars and Capacity Building II	PI	$178,570
51. MIT Lincoln Labs	6/1/2018-5/30/2020	IoT Testbed Development and Common DSP Function Implementation	PI	$300,000
52. NSF (Dartmouth Subaward)	10/1/2018-9/30/2019	Secure and Trustworthy Cyberspace	PI	$243,000
53. NSF SaTC Frontier	10/01/2020-09/30/2025	Security and Privacy in the Lifecycle of IoT for Consumer Environments (SPLICE)	Co-PI	$10,000,000 ($1,387,000)
54. ARLIS (UMD Subaward)	09/01/2020-08/31/2021	NBIoT Testbed Development	PI	$100,000
55. NSA/GTRI	09/01/2021-present	Connected Car Security	PI	$1,200,000
56. NASA JPL	03/01/2020-08/28/2020	Specification-based Anomaly Detection for Embedded Devices	PI	$40,000
57. DoD/NSA	08/24/2020-08/31/2021	DoD Cybersecurity Scholarship: CREAM Scholars and Capacity Building	PI	$146,555
58. Autodesk	06/01/2020-12/11/2020	IoT Vulnerability Assessment Tool	PI	$30,000

59. ARLIS	09/01/2020-08/31/2021	5G Testbed Development	PI	$150,000
60. NSF	07/01/2021-06/30/2026	CyberCorps Scholarship for Service: Secure Embedded Systems Scholarship Program	PI	$3,184,625
61. DoD/NSA	09/15/2021	DoD Cybersecurity Scholarship Program	PI	$68,735
62. Keysight	09/2021	Monetary Gift	PI	$20,000
63. Keysight	09/15/2021	Equipment Gift	PI	$160,000
64. Shift5	11/15/2021	Monetary Gift	PI	$50,000
65. Autodesk	11/01/2021	IoT Security Capstone Project	PI	$43,000
66. Cadence	06/2022	Monetary Gift	PI	$50,000
67. Maryland Industrial Partnerships	07/01/2022-06/30/2023	VISPR: A Verified Instruction Secure Processor Design for Trustworthy Code Execution	PI	$100,000
68. BAA # ("S2MARTS Project No. 22-16")	06/01/2023-505/31/2028	SCALE: A Microelectronic Workforce Development Project	PI	$500,000
69. NSA/GTRI	05/23/2021-09/30/2024	Autonomous Defensive Cyber Operations (DCO) Research & Development (R&D)	PI	$1,057,914
70. Intel University Research & Collaboration Office	11/21/2023	Monetary Gift Development of a System-on-Chip (SoC) Tape Out Course	PI	$50,000
71. Morgan State University Office of Technology Transfer	11/01/2023-10/31/2024	Smart Home Security System	PI	$50,000

VIII. Presentations

1. "Future Directions of SiC Research at Purdue," *NASA Lewis Research Center*, Cleveland, OH, Nov. 10, 1994.
2. "VLSI Research at Purdue," *Indiana Microelectronics Center*, October 26, 1995.
3. "Design of a High-Performance Chip for Scheduling Real-Time Traffic in ATM Networks," *National Semiconductor Corporation*, Santa Clara, CA, March 4-5, 1996.
4. "Design of Smart Power ICs using Silicon Carbide Technology," *IEEE Computer Society VLSI Workshop*, Clearwater Beach, FL, November 5, 1996.
5. "Design of an Ultrafast Optical Processing Chip," *IEEE Computer Society VLSI Workshop*, Clearwater Beach, FL, Nov. 5, 1996.
6. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *Cornell EE Colloquium Series*, April 8, 1997.
7. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *Princeton EE Colloquium Series*, May 12, 1997.
8. "Microelectronic Processing of SiC CMOS Devices," *MIT Material Science and Engineering Electronic Materials Seminar*, September 18, 1997.
9. "Development of 6H-SiC CMOS Technology and its Applications to Power Electronic Building Blocks (PEBBs)," *MIT Microsystems Technology Lab VLSI Seminar Series*, October 28, 1997.
10. "Design Issues in Power Electronics Building Block (PEBB) System Integration," *IEEE Workshop on VLSI*, Orlando, FL, April 15,1998.
11. "Recent Advances in Silicon Carbide Circuit Technology," *DARPA Defense Science Research Council Meeting on Harsh Environments*, System Planning Center, Arlington, VA, May 7, 1998.
12. "Integrated Electronics for Harsh Environments," *DARPA MEMS for Harsh Environments Workshop*, Dulles, VA, Oct. 23-24, 1998.
13. "Integrated MEMS for Harsh Environments," Berkeley Sensors and Actuators Center Seminar - University of California at Berkeley, Berkeley, CA, April 12, 1999.
14. "Silicon Carbide Circuit Technology and Applications," Integrated Circuits Technology and Design Seminar - Stanford University, Palo Alto, CA, May 11, 1999.
15. "Integrated MEMS for Harsh Environments," MiRC GaTech School of ECE, March 23, 2001.
16. "Integrated MEMS for Harsh Environments," IT Constellation Seminar, RPI, March 20, 2002.
17. "The Roadmap to Single-Chip WCDMA Transceivers – A Circuit Designer's Perspective," Symbol Technologies Distinguished Lecture, Polytechnic University, April 9, 2002.
18. "CBCRL Research Highlights," Columbia University EE VLSI Seminar Series, Dec.15, 2003.
19. "CBCRL Research Highlights," Analog Devices, Wilmington, MA, July 12, 2004.
20. "High Performance VCO Design using SiGe BiCMOS Technology," IEEE Electron Devices Society Distinguished Lecture, Raytheon, Tampa, FL, Sept. 29, 2004.

21. Keynote Speaker, "IoT Device Security Research at Morgan State University," Center for Embedded Systems and for Critical Applications Annual Meeting, Va Tech ECE Department, April 23, 2016.
22. Keynote Speaker, 4th Annual Cybersecurity Conference for Executives, Johns Hopkins University Information Security Institute, Sept. 19, 2017.
23. Invited Speaker, "Cream Research & Education: Enabling the Next Generation Cybersecurity Workforce," Intelligence Community Academic Research Symposium, National Academy of Sciences, Washington, DC, Sept. 26, 2017.
24. Invited Speaker, "Applications of AI in Cybersecurity," SIAM International Conference on Data Mining, Virtual, April 29, 2021.
25. Invited Speaker, "Research Highlights in the Cybersecurity Assurance & Policy Center," Science and Technology in International Affairs at the Edmond A. Walsh School of Foreign Service, Georgetown University, October 4, 2021.
26. Invited Speaker, "Research Highlights in the Cybersecurity Assurance & Policy Center," Center for Automotive Research (CAR), Ohio State University, College of Engineering, Oct. 12, 2021.
27. DARP ERI Summit Workshop, "What is a new approach to workforce development and why will it be successful?", Aug. 24, 2023, Seattle, WA.
28. Purdue-IMEC Creating a Whole-of-Nation Approach to CHIPS Act Objectives for Education and Innovation Workshop panel entitled "Developing a Domestic Workforce to Fuel Semiconductor Industry Resurgence", Nov. 3, 2023, Washington, DC.

IX. Service

A. Professional Contributions

Administrative:

- NIST IoT Advisory Board, January 2023 – present.
- ScienceMakers Advisory Committee, May 2020 – present.
- National Academy of Sciences Intelligence Community Science Board Cybersecurity Committee, September 2018 to present.
- State of Maryland Cybersecurity Council, June 2016 to present.
- NSF Panel, Electrical, Communications and Cyber Systems Division, April 2018.
- NSF Panel, Electrical, Communications and Cyber Systems Division, April 2014, 2016.
- NSF CAREER Panel, Electrical, Communications and Cyber Systems Division, Fall 2013, 2014.
- National Research Council Assessment Panel of the NIST Program – Semiconductor Electronics Panel Member, 2007-2009.
- IEEE Solid State Circuits Society Administrative Committee Member, 2007-2009.
- Organizing Committee, 6th and 7th German-American Symposium on Frontiers of Engineering, National Academy of Engineering.
- AdCom Member, IEEE Electron Device Society Educational Activities Committee, 2000 - present. IEEE Electron Devices Society Distinguished Lecturer, 2000- 2005.
- IEEE Electron Devices Society AdCom Education Activities Committee, 2000-2005.
- Co-Organizer, DARPA Workshop on MEMS for Harsh Environments, 1998.

Technical Program Committees:

- IEEE Symposium on VLSI Technology and Circuits, 2023 – present.
- Hot Topics in the Science of Security (HOTSOS) Symposium, 2020 – present.
- IEEE Applied Imagery Pattern Recognition (AIPR) Workshop: Trusted Computing, Privacy, and Securing Multimedia, 2020 – present.
- USENIX Security Symposium 2021 – present.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2020 – present.
- IEEE Secure Development Conference (SECDEV), 2020 – present.
- IEEE Physical Assurance and Inspection of Electronics (PAINE), 2020 – present.
- IEEE International Hardware Oriented Security and Trust Symposium, 2016 – present.
- IEEE International Solid State Circuits Conference (ISSCC), 2005 – 2006.
- IEEE Custom Integrated Circuits Conference (CICC), 2005 – 1007.
- IEEE International Symposium on Circuits and Systems (ISCAS), 2004 – present.
- IEEE Bipolar/BiCMOS Circuits Technology Meeting (BCTM), 2004 – 2007.
- IEEE Compound Semiconductor IC (CSICS) Symposium, 2004.
- IEEE Radio Frequency IC (RFIC) Symposium, 2003 – 2006.
- IEEE Computer Society Symposium on VLSI, 2003 – present.
- ACM International Symposium on Low Power Electronics and Design (ISLPED), 2003 - present.
- IEEE International Microwave Symposium, 2003, 2008.
- International Conf. on Microelectronic Systems Education, 2003.
- IEEE Great Lakes Symposium on VLSI, 2003.
- IEEE Sensors, 2002, 2003.
- IEEE Symposium on Power Semiconductors and Devices, 2001-2003.
- IEEE Asian and South Pacific Design Automation Conference,1999.
- IEEE Industry Applications Society Annual Meeting, 1998.
- IEEE International Test Conference, 1993 - 1996.
- IEEE Computer Society Workshop on VLSI, 1995.

Editorial Service:

- Editorial Board, The BRIDGE magazine of IEEE Eta Kappa Nu, 2021 - present.
- Editorial Board, Journal of Hardware and Systems Security, 2017-present.
- Assoc. Editor, IEEE *TCAS-II*, 2008-2010.
- Editorial Advisory Board of *Science Spectrum Magazine*, 2005.
- Guest Editor, Special Issue of the IEEE *Journal of Solid-State Circuits*: Compound Semiconductor IC Symposium, 2005.
- Editor, IEEE *Electron Device Letters*, 2003-2006.

University Contributions:

- Lead Development of Secure Embedded Systems Ph.D. program.
- Director, Cybersecurity Assurance and Policy (CAP) Center
- Director, Center for Reverse Engineering and Assured Microelectronics (CREAM) Lab
- Co-Director of NSA/DHS Center for Academic Excellence in Cyber Defense Education
- Leadership and coordination of all university cybersecurity research activities and initiatives.

- Chair, Faculty Recruitment Committee, ECE Department.
- Graduate Committee Member, ECE Department.

B. Other Contributions

Reviewer, ACM Transactions on Computing for Healthcare, 2020.

- Reviewer, National Cyber Summit, 2018.
- Reviewer, IEEE *Microwave and Wireless Component Letters*, 2002 – present (12 papers)
- Reviewer, IEEE *Microwave Theory and Techniques*, 2002 – present
- Reviewer, IEEE *Transactions on Circuits and Systems*, 2000 – present
- Reviewer, IEEE *Transactions on Electron Devices*, 2000 – present (22 papers)
- Reviewer, IEEE *Electron Device Letters*, 1996 – present (24 papers)
- Reviewer, IEEE *Journal of Solid-State Circuits*, 1992 – present (31 papers)
- Reviewer, National Science Foundation CISE, ENG, ERC, 1995 - present (65 proposals)

Consulting Experience

2003 – 2012, Future Trends Forum, Madrid, Spain.
2003 – 2012, Institute for Defense Analysis, Alexandria, VA.
2001, IBM Communications Research and Development Center, Yorktown Heights, NY.
1998, Irell & Manella LLP, Los Angeles, CA.
1998, DARPA-Defense Science Research Council, Arlington, VA.
1997, Foster-Miller, Waltham, MA.